DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
2SK3304

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3304 is N-Channel MOS FET device that features a Low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply.

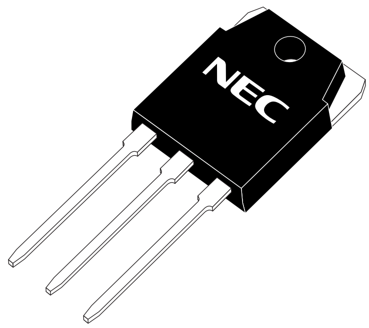
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3304	TO-3P

FEATURES

- Low gate charge :
  Q_G = 44 nC TYP. (V_{DD} = 450 V, V_{GS} = 10 V, I_D = 7.0 A)
- Gate voltage rating : ±30 V
- Low on-state resistance :
  $R_{DS(on)}$ = 2.0 Ω MAX. (V_{GS} = 10 V, I_D = 4.0 A)
- Avalanche capability ratings

(TO-3P)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	900	V
Gate to Source Voltage	$V_{GSS(AC)}$	±30	V
Drain Current (DC)	$I_{D(DC)}$	±7	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±21	A
Total Power Dissipation (T_C = 25°C)	P_T	130	W
Total Power Dissipation (T_A = 25°C)	P_T	3.0	W
Storage Temperature	T_{stg}	–55 to + 150	°C
Single Avalanche Current Note2	I_{AS}	7	A
Single Avalanche Energy Note2	E_{AS}	147	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 V → 0 V

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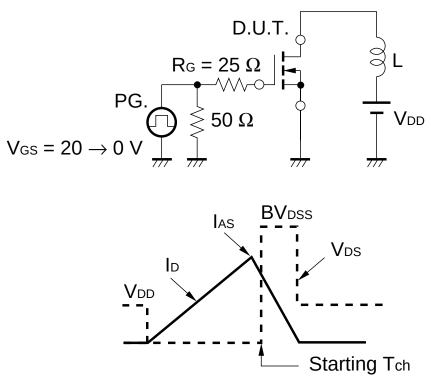
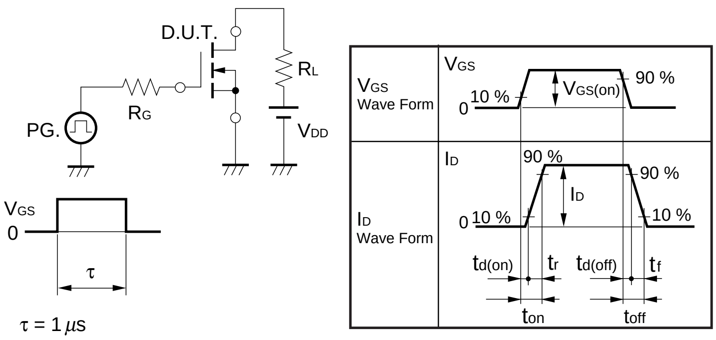
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I_{DSS}	V_{DS} = 900 V, V_{GS} = 0 V			100	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1.0 mA	2.5		3.5	V
Forward Transfer Admittance	$\| y_{fs} \|$	V_{DS} = 20 V, I_D = 4.0 A	2.5	4.7		S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4.0 A		1.6	2.0	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V V_{GS} = 0 V f = 1 MHz		1300		pF
Output Capacitance	C_{oss}			240		pF
Reverse Transfer Capacitance	C_{rss}			55		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 150 V I_D = 4.0 A $V_{GS(on)}$ = 10 V R_G = 10 Ω, R_L ≅ 36 Ω		20		ns
Rise Time	t_r			44		ns
Turn-off Delay Time	$t_{d(off)}$			73		ns
Fall Time	t_f			45		ns
Total Gate Charge	Q_G	V_{DD} = 450 V V_{GS} = 10 V I_D = 7.0 A		44		nC
Gate to Source Charge	Q_{GS}			6		nC
Gate to Drain Charge	Q_{GD}			28		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 7.0 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 7.0 A, V_{GS} = 0 V di/dt = 50 A/μs		2.4		μs
Reverse Recovery Charge	Q_{rr}			13.5		μC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

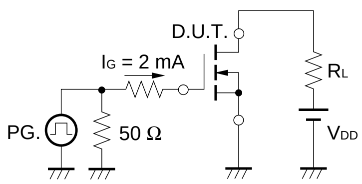


TEST CIRCUIT 2 SWITCHING TIME



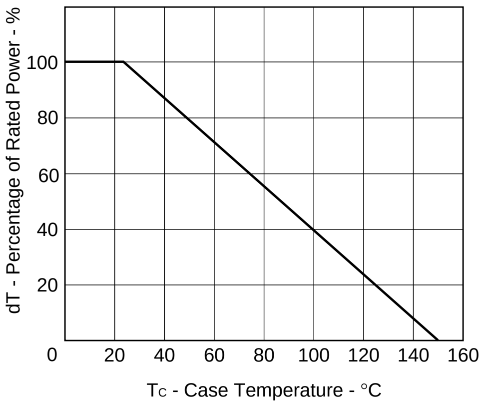
τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 3 GATE CHARGE

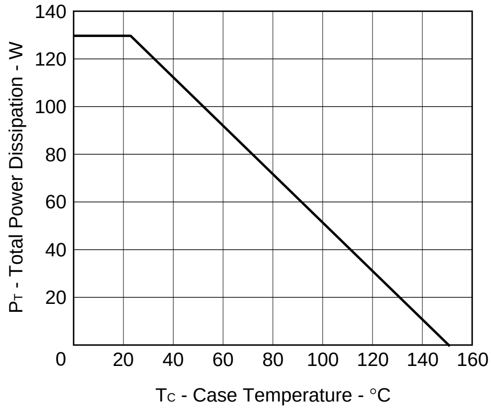


TYPICAL CHARACTERISTICS (T_A = 25 °C)

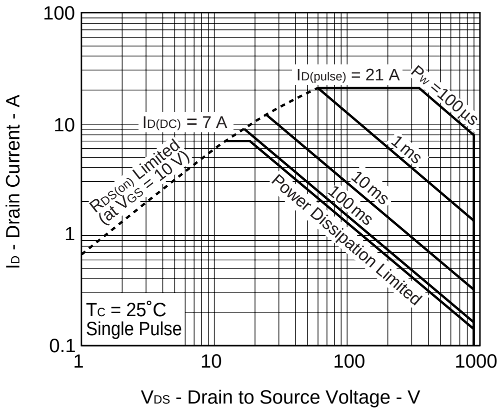
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



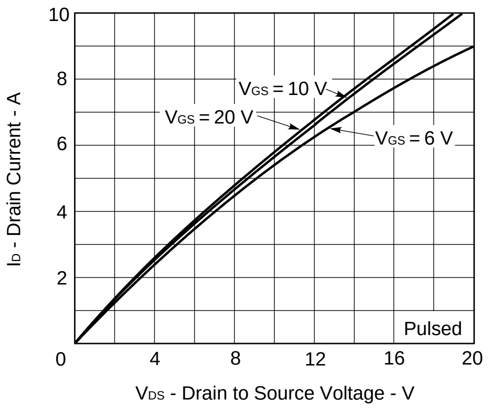
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



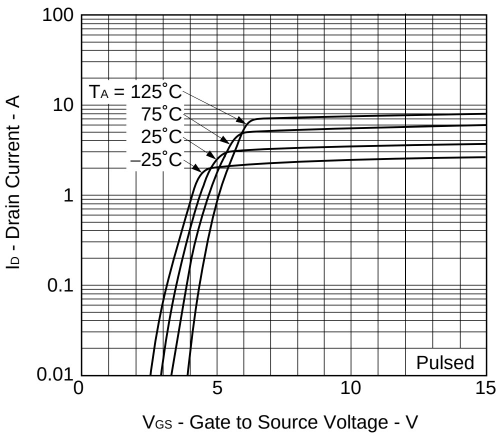
FORWARD BIAS SAFE OPERATING AREA

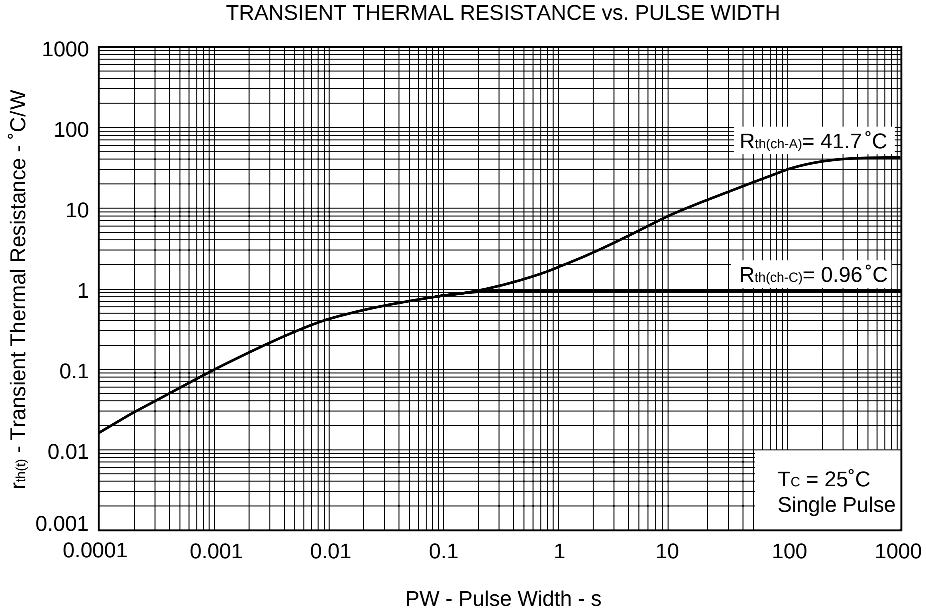


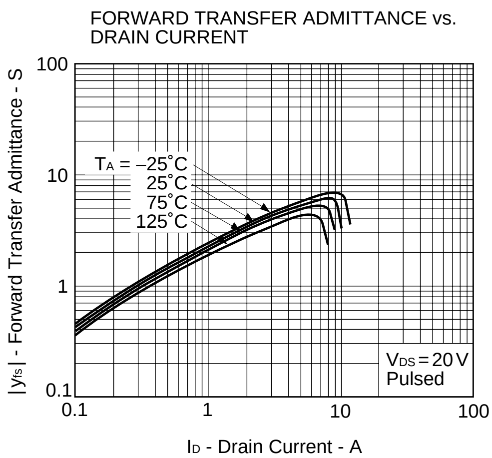
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

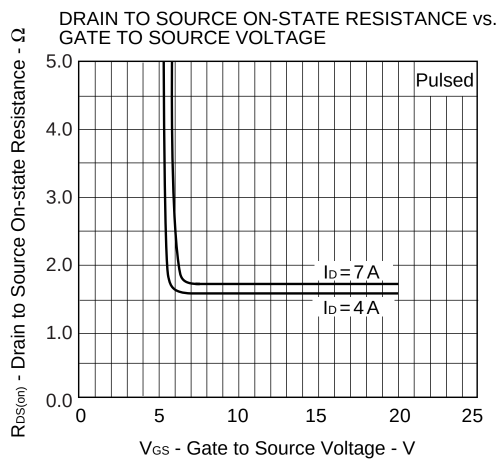


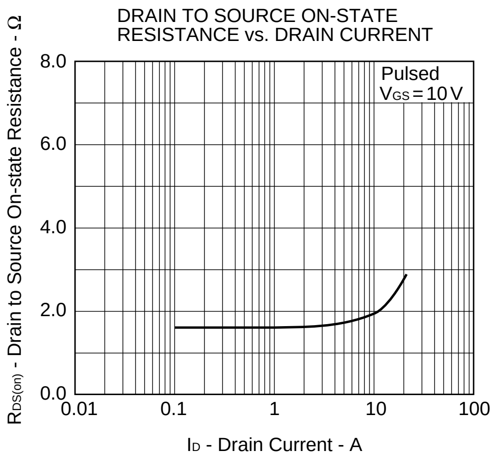
FORWARD TRANSFER CHARACTERISTICS

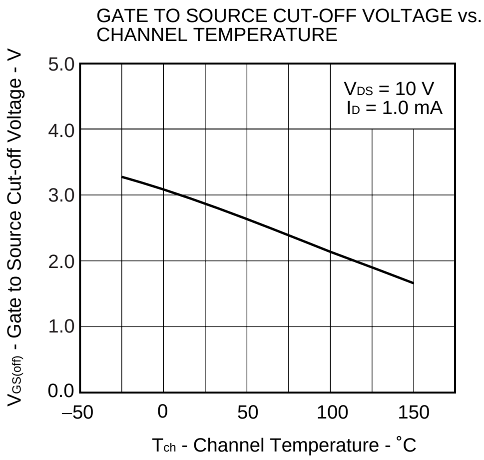


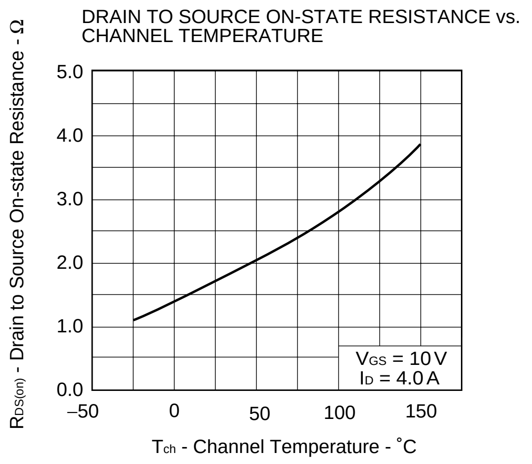

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH
$r_{th(t)}$ - Transient Thermal Resistance - ˚C/W
$R_{th(ch-A)}$= 41.7˚C
$R_{th(ch-C)}$= 0.96˚C
T_C = 25˚C
Single Pulse
1000
100
10
1
0.1
0.01
0.001
0.0001
0.001
0.01
0.1
1
10
100
1000
PW - Pulse Width - s

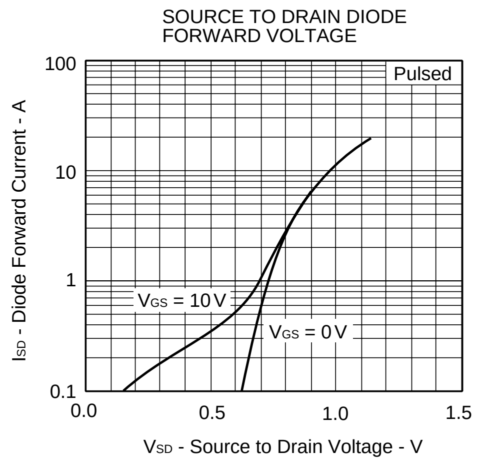

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT
|y_{fs}| - Forward Transfer Admittance - S
T_A = −25˚C
25˚C
75˚C
125˚C
V_{DS} = 20 V
Pulsed
100
10
1
0.1
0.1
1
10
100
I_D - Drain Current - A

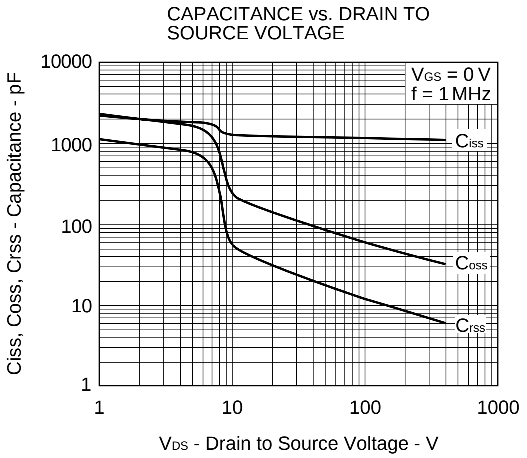

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE
$R_{DS(on)}$ - Drain to Source On-state Resistance - Ω
Pulsed
I_D = 7 A
I_D = 4 A
5.0
4.0
3.0
2.0
1.0
0.0
0
5
10
15
20
25
V_{GS} - Gate to Source Voltage - V

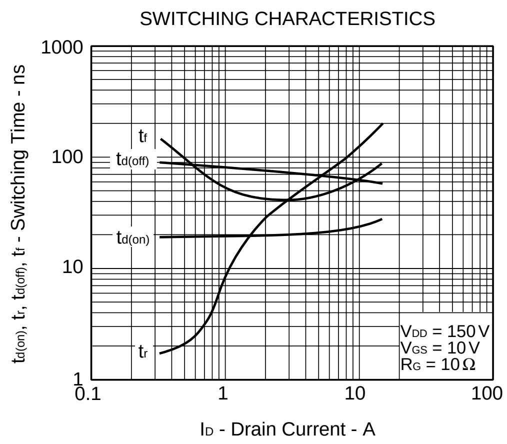

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT
$R_{DS(on)}$ - Drain to Source On-state Resistance - Ω
Pulsed
V_{GS} = 10 V
8.0
6.0
4.0
2.0
0.0
0.01
0.1
1
10
100
I_D - Drain Current - A

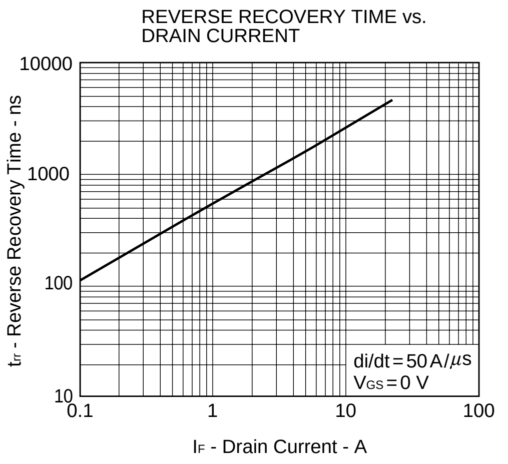

GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE
$V_{GS(off)}$ - Gate to Source Cut-off Voltage - V
V_{DS} = 10 V
I_D = 1.0 mA
5.0
4.0
3.0
2.0
1.0
0.0
−50
0
50
100
150
T_{ch} - Channel Temperature - ˚C

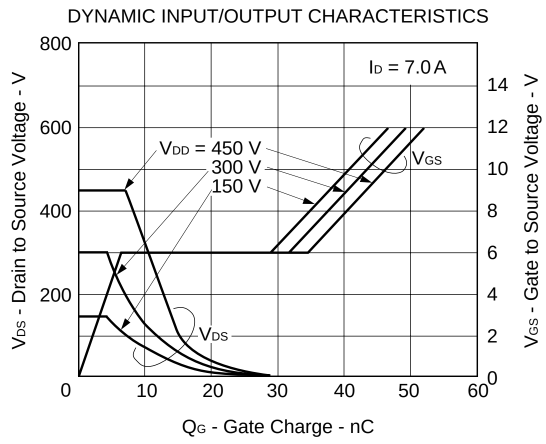

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE
RDS(on) - Drain to Source On-state Resistance - Ω
5.0
4.0
3.0
2.0
1.0
0.0
–50
0
50
100
150
VGS = 10 V
ID = 4.0 A
Tch - Channel Temperature - ˚C


SOURCE TO DRAIN DIODE
FORWARD VOLTAGE
ISD - Diode Forward Current - A
100
10
1
0.1
0.0
0.5
1.0
1.5
Pulsed
VGS = 10 V
VGS = 0 V
VSD - Source to Drain Voltage - V

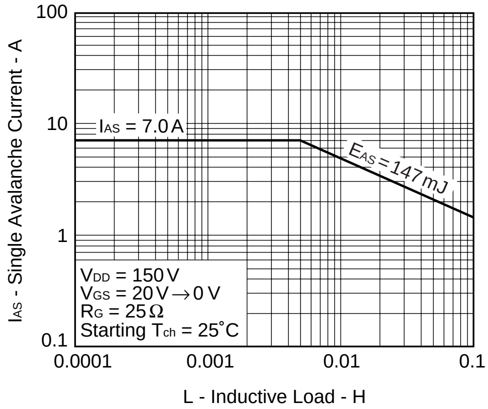

CAPACITANCE vs. DRAIN TO
SOURCE VOLTAGE
Ciss, Coss, Crss - Capacitance - pF
10000
1000
100
10
1
1
10
100
1000
VGS = 0 V
f = 1 MHz
Ciss
Coss
Crss
VDS - Drain to Source Voltage - V


SWITCHING CHARACTERISTICS
td(on), tr, td(off), tf - Switching Time - ns
1000
100
10
1
0.1
1
10
100
tf
td(off)
td(on)
tr
VDD = 150 V
VGS = 10 V
RG = 10 Ω
ID - Drain Current - A

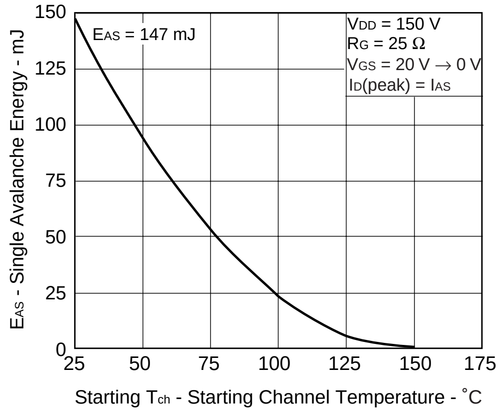

REVERSE RECOVERY TIME vs.
DRAIN CURRENT
trr - Reverse Recovery Time - ns
10000
1000
100
10
0.1
1
10
100
di/dt = 50 A/μs
VGS = 0 V
IF - Drain Current - A


DYNAMIC INPUT/OUTPUT CHARACTERISTICS
VDS - Drain to Source Voltage - V
800
600
400
200
0
10
20
30
40
50
60
ID = 7.0 A
VDD = 450 V
300 V
150 V
VGS
VDS
14
12
10
8
6
4
2
0
VGS - Gate to Source Voltage - V
QG - Gate Charge - nC

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

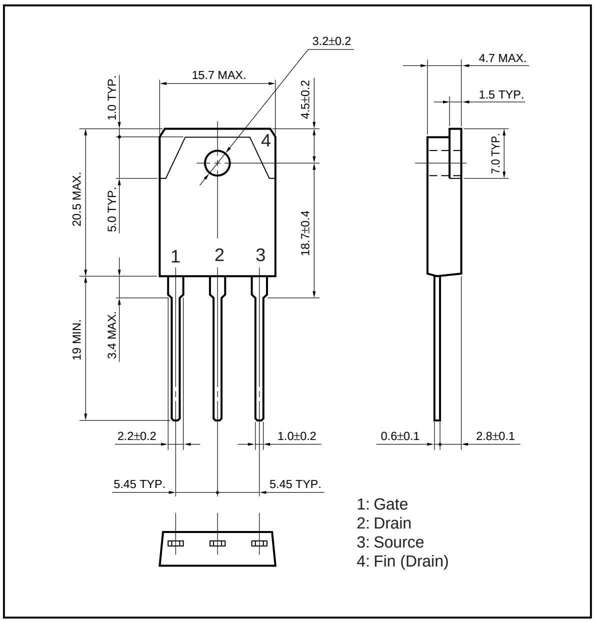


SINGLE AVALANCHE ENERGY vs STARTING CHANNEL TEMPERATURE

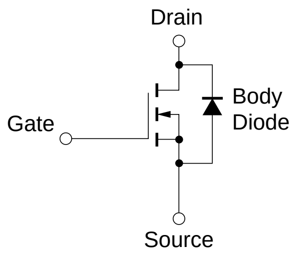


PACKAGE DRAWING (Unit : mm)

TO-3P (MP-88)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.